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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/050,004	01/14/2002	Mian Smith	015114-054000US	5525

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EXAMINER
TRA, ANH QUAN

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 06/30/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/050,004	SMITH ET AL.	
	Examiner	Art Unit	
	Quan Tra	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 May 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10,12-19 and 21-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *21-28* is/are allowed.

6)☒ Claim(s) *1,5,7 and 12* is/are rejected.

7)☒ Claim(s) *2-4,6, 8-10 and 13-19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *5* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

This office action is in response to the amendment filed 05/13/2003. A new ground of rejection is introduced.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 7 and 12 are rejected under 35 U.S.C. 102(b) as being anticipated by Utsunomiya et al. (USP 5905291).

As to claim 1, Utsunomiya et al. discloses in figure 10 a charge pump circuit comprising: a first native transistor (14) (column 7, lines 60-65, teaches that transistor M14 having threshold value approximately to 0 V, applicant's response in the Remarks admitted that native transistor as a low threshold voltage (e.g., 0.3 Volts or less)) first depletion transistors (M15-M28)each having a threshold voltage that is lower that a threshold voltage of the first native transistor at a common source voltage (column 7, lines 60-65), wherein the first native transistor and the first depletion transistors are coupled together in series between an input and an output of the charge pump circuit; and first capacitors (C1-C28), wherein each of the first depletion transistors is coupled to one of the first capacitors, first subset of the first capacitors (odd number of capacitors) are coupled to receive a first clock signal (Φ), and second subset of the first capacitors are coupled to receive a second clock signal (Φ*).

As to claim 7, figure 10 further shows a second native transistor (M14) coupled in series with the first native transistor.

As to claim 12, figure 10 shows a method for receiving an input voltage and providing a boosted output voltage, the method comprising: boosting the input voltage by applying a first clock signal (Φ) to a drain of a first native transistor (M14); boosting a source voltage of the first native transistor by applying the first clock signal and a second clock signal (Φ*) to a drain and source of each of a first set of depletion transistors (M15-M28) that are coupled together in series to provide output voltage, the first set of depletion transistors each having a threshold voltage that is lower than a threshold voltage of the first native transistor at a common source voltage.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hsu et al. (USP 5978283) (Applicant's ISD) in view of Ulsunomiya et al. (USP 5905291).

Hsu et al's figure 1 shows a charge pump circuit having plurality of transistors (A1-A8) connected in series; plurality of capacitors (C1-C8) respectively connected to the plurality of transistors (A1-A8); and plurality of diode connected transistors (M1-M8) respectively connected to the gate of the plurality of transistors (A1-A8). Thus, figure 1 shows all limitations of the claim except for the charge pump having two stages, wherein the first stage comprising

native transistors and the second stage comprising depletion transistors. However, Ulsunomiya et al.'s figure 10 shows charge pump circuit having two stages (M1-M14 and M15-M28) comprising native transistors and depletion transistors respectively. The circuit having the advantage of having high function, high efficiency, and low cost (column 1, lines 25-35). Therefore, it would have been obvious to one having ordinary skill in the art to modify Hsu et al.'s charge pump circuit with two stages comprising native transistors and depletion transistors respectively for the purpose of having a high function, high efficiency, and low cost charge pump circuit.

Allowable Subject Matter

5. Claims 2-4, 6, 8-10 and 13-19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. Claims 21-28 are allowed.

Claims 2-4, 6, 8-10, 13-19 would be and claims 21-28 are allowable because the prior art fails to teach or suggest a circuit (such as figure 3) having a native transistor, first and second set of depletions transistors, wherein the second set of depletion transistors each having threshold voltage that is lower than the threshold voltage of each of the first set of depletion transistors at a common source voltage.

Claim 10 would be allowable because the prior art fails to teach or suggest third native transistors, wherein a gate, the drain, and a source of each of the first depletion transistors are coupled to one of the third native transistors.

Response to Arguments

A new ground of rejection is introduced above. Therefore, there is no response to Applicant's arguments.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The reference is cited as interest because it shows circuit analogous to the claimed invention.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 703-308-6174. The examiner can normally be reached on 8:00 A.M.-5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 703-308-4876. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

QT
June 16, 2003

Terry D. Cunningham
Primary Examiner